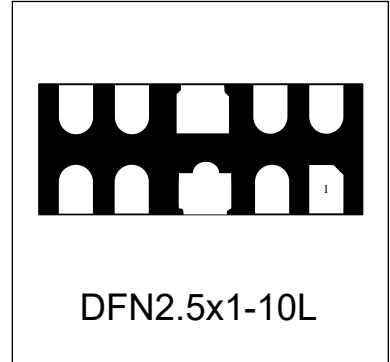




## Features

- Solid-state silicon-avalanche technology
- Low operating and clamping voltage
- Up to four I/O Lines of Protection
- Ultra low capacitance: 0.3pF typical(I/O to I/O)
- Low Leakage
- Low operating voltage:5V
- Flow-Through design



## IEC Compatibility (EN61000-4)

- IEC 61000-4-2 (ESD)  $\pm 18\text{kV}$  (air),  $\pm 12\text{kV}$  (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 5A (8/20 $\mu\text{s}$ )

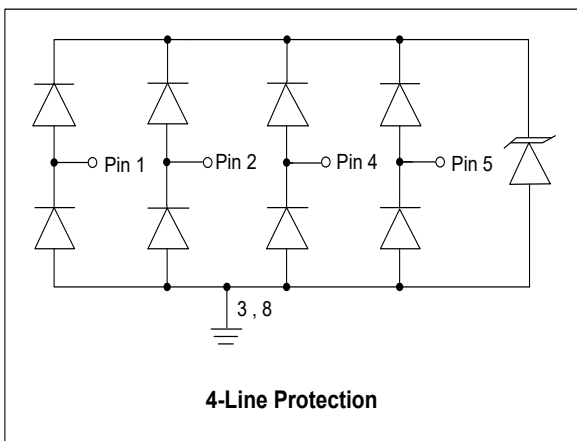
## Mechanical Characteristics

- DFN-10L package (2.5 $\times$ 1.0 $\times$ 0.50mm)
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code
- Packaging: Tape and Reel
- RoHS Compliant

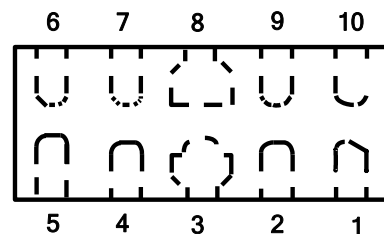
## Applications

- Digital Visual Interface(DVI)
- MDDI Ports
- DisplayPort TM Interface
- PCI Express
- High Definition Multi-Media Interface(HDMI)
- eSATA Interfaces

## Circuit Diagram



## Schematic & PIN Configuration



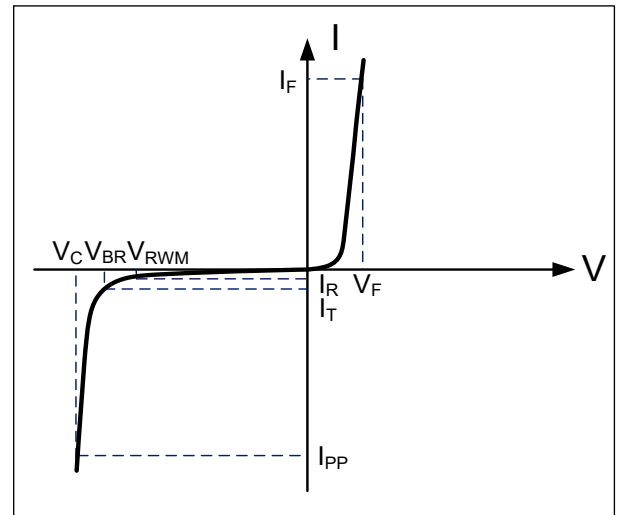
Pin	Identificaion
1,2,4,5	Input Lines
6,7,9,10	Output Lines (No Internal Connection)
3,8	Ground

## Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{PP}$	100	Watts
Peak Pulse Current ( $t_p = 8/20\mu s$ )	$I_{pp}$	5	A
ESD per IEC 61000-4-2(Air)	$V_{ESD}$	+/-18	kV
ESD per IEC 61000-4-2(contact)		+/-12	
Operating Temperature	$T_J$	-55 to + 125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

## Electrical Parameters (T=25°C )

Symbol	Parameter
$I_{PP}$	Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$



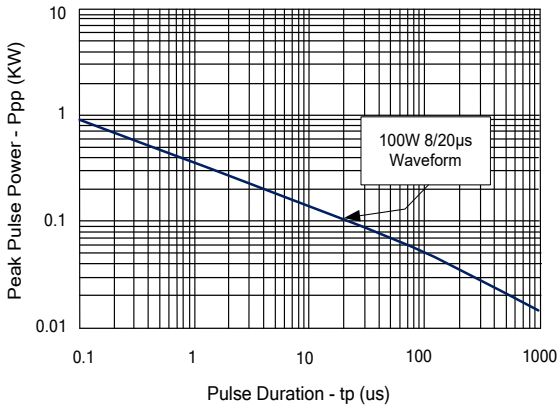
## Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$	Any I/O pin to ground			5.0	V
Reverse Breakdown Voltage	$V_{BR}$	$I_T = 1mA$ Any I/O pin to ground	6.0			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5V, T=25°C$ Any I/O pin to ground			1	$\mu A$
Clamping Voltage	$V_C$	$I_{pp}=1A, t_p=8/20\mu s$ Any I/O pin to ground			9	V
Clamping Voltage	$V_C$	$I_{pp}=5A, t_p=8/20\mu s$ Any I/O pin to ground			15	V
Junction Capacitance	$C_j$	$V_R = 0V, f = 1MHz$ I/O pin to GND			0.8	pF
		$V_R = 0V, f = 1MHz$ Between I/O pins		0.3	0.4	pF

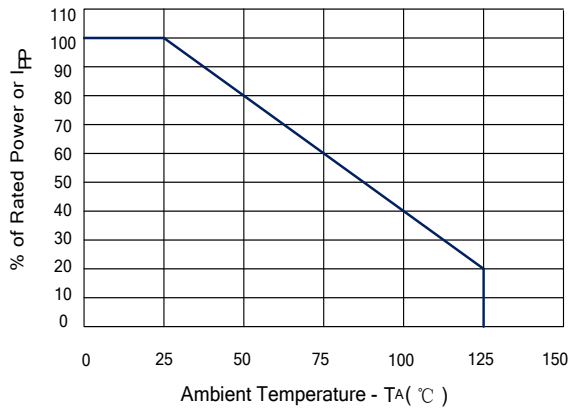


### Typical Characteristics

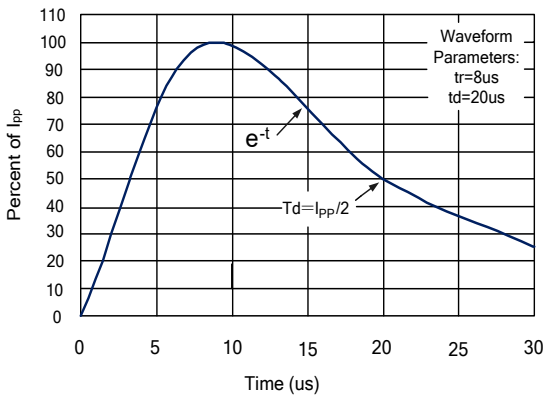
Non-Repetitive Peak Pulse Power vs. Pulse Time



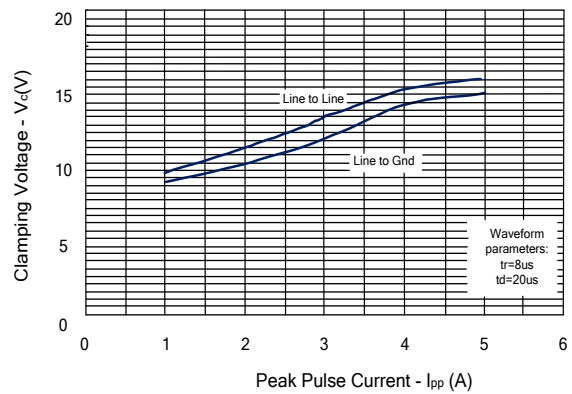
Power Derating curve



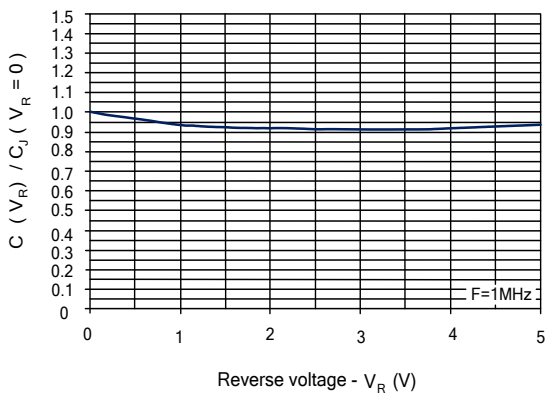
Pulse Waveform



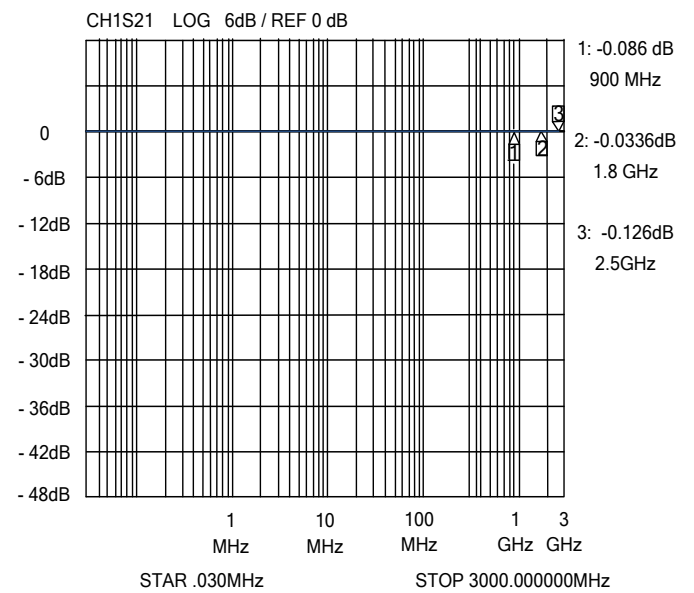
Clamping Voltage vs. Peak Pulse Current



Normalized Capacitance vs. Reverse Voltage



Insertion Loss S21 - I/O to GND



## Application Information

### Design Recommendations for HDMI protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capacitance. Furthermore, adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The DW05-4R2P-S and DW05-2R2P-S are specifically designed for protection of high-speed interfaces such as HDMI. They present <math><0.4\text{pF}</math> capacitance between the pairs while being rated to handle  $\pm 8\text{kV}$  ESD contact discharges ( $\pm 15\text{kV}$  air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless SLP package that is less than 1.1mm wide. They are designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes even more critical as signal speeds increase.

### Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the DW05-4R2P-S. The solid line represents the PCB trace. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines connected at pins 2, 4, and 5 also. Ground is connected at pins 3 and 8. One large ground pad should be used in lieu of two separate pads. The same layout rules apply for the DW05-2R2P-S.

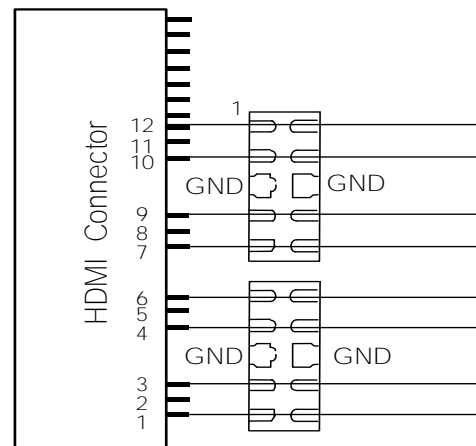


Figure 1. Flow through layout Using **DW5-4R2P-S**

### Layout Guidelines for Optimum ESD Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible. This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible. Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.

## Application Information (cont)

### Protecting MDDI Ports with DW05-4R2P-S and DW05-2R2P-S

The small package size and low capacitance of the DW05-4R2P-S and DW05-2R2P-S make them ideal for high-speed lines in portable applications. One such application is the protection of MDDI ports in cellular phones. MDDI is a serial data interface operating at 480Mb/s per line pair. The lines are scalable for increased speed and display resolution. A MDDI port protection example is shown in Figure 5. The DW05-4R2P-S is used to protect two differential line pairs while an DW05-2R2P-S is used to protect the MDDI strobe lines. Note that devices are used on both the main board and LCD side of the MDDI port. Devices on the main board are needed to protect the MDDI controller in the Base band processor and devices on the LCD board to protect MDDI controller in LCD module. A single line TVS such as the WE05D5 is used to protect the MDDI power line. The protection devices should be placed close to the connector of each board. Traces are routed directly through each device, minimizing parasitic inductance. Connections to the ground plane should be made with multiple micro vias when possible.

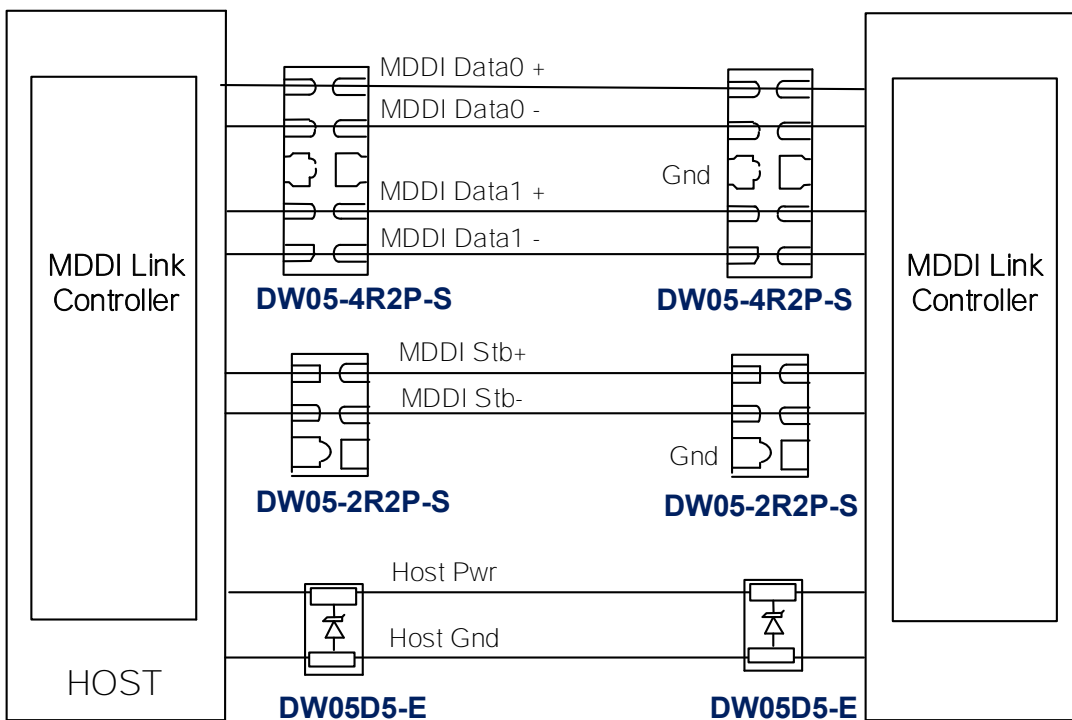


Figure 2.MDDI Port Protection



Outline Drawing –DFN-10L

PIN1 INDICATOR (LASER MARK)

SEATING PLANE

NOTES:  
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

DFN2.5x1-10L

DIMENSIONS

DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.017	.020	.022	0.45	0.50	0.55
A1	.000	.001	.002	0.00	0.02	0.05
A2	(.006)			(0.15)		
b	.006	.008	.010	0.15	0.20	0.25
b1	.014	.016	.018	0.35	0.40	0.45
b2	.008	.010	.018	0.20	0.25	0.45
D	.096	.098	.100	2.45	2.50	2.55
E	.037	.039	.041	0.95	1.00	1.05
e	.020 BSC			0.50 BSC		
L	.014	.016	.018	0.35	0.40	0.45
L1	.000	.003	.004	0.00	0.075	0.10
L2	.000	.002	.003	0.00	0.05	0.08
h	.000	.005	.006	0.00	0.12	0.15
N	8			8		
aaa	0.003			0.08		
bbb	0.004			0.10		

DIMENSIONS

DIM	INCHES	MILLIMETERS
C	(.034)	(0.875)
G	.008	0.20
P	.020	0.50
P1	.039	1.00
X	.010	0.25
X1	.018	0.45
Y	.027	0.675
Y1	(.061)	(1.55)
Z	.061	1.55

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.

CONSULT YOUR MANUFACTURING TO ENSURE YOUR COMPANYS MANNUFACTURING GUIDELINES ARE MET.

Marking Codes

Part Number	DW05-4R2P-S	Marking Code	5R2P or 5UE
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Package Information

Qty: 3k/Reel